ANALOG DEVICES

Single Supply, Rail-to-Rail Low Power FET-Input Op Amp

AD822

FEATURES

TRUE SINGLE SUPPLY OPERATION
- Output Swings Rail to Rail
- Input Voltage Range Extends Below Ground
- Single Supply Capability from +3 V to +36 V
- Dual Supply Capability from ±1.5 V to ±18 V

HIGH LOAD DRIVE
- Capacitive Load Drive of 350 pF, G = 1
- Minimum Output Current of 15 mA

EXCELLENT AC PERFORMANCE FOR LOW POWER
- 800 µA Max Quiescent Current per Amplifier
- Unity Gain Bandwidth: 1.8 MHz
- Slew Rate of 3.0 V/µs

GOOD DC PERFORMANCE
- 800 µV Max Input Offset Voltage
- 2 µV/°C Typ Offset Voltage Drift
- 25 pA Max Input Bias Current

LOW NOISE
- 13 nV/√Hz @ 10 kHz

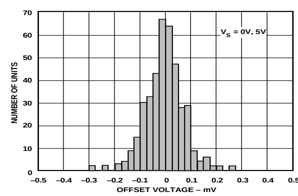
NO PHASE INVERSION

APPLICATIONS

- Battery Powered Precision Instrumentation
- Photodiode Preamps
- Active Filters
- 12- to 14-Bit Data Acquisition Systems
- Medical Instrumentation
- Low Power References and Regulators

CONNECTION DIAGRAM

8-Pin Plastic DIP, Cerdip and SOIC



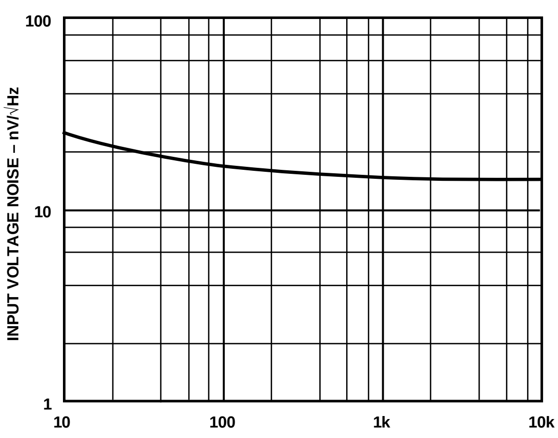
PRODUCT DESCRIPTION

The AD822 is a dual precision, low power FET input op amp that can operate from a single supply of +3.0 V to 36 V, or dual supplies of ±1.5 V to ±18 V. It has true single supply capability with an input voltage range extending below the negative rail, allowing the AD822 to accommodate input signals below ground in the single supply mode. Output voltage swing extends to within 10 mV of each rail providing the maximum output dynamic range.

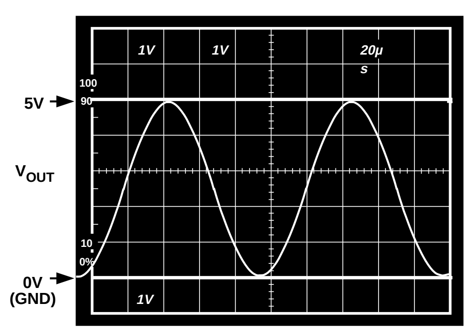
Offset voltage of 800 µV max, offset voltage drift of 2 µV/°C, input bias currents below 25 pA and low input voltage noise provide dc precision with source impedances up to a Gigaohm. 1.8 MHz unity gain bandwidth, –93 dB THD at 10 kHz and 3 V/µs slew rate are provided with a low supply current of 800 µA per amplifier. The AD822 drives up to 350 pF of direct capacitive load as a follower, and provides a minimum output current of 15 mA. This allows the amplifier to handle a wide range of load conditions. This combination of ac and dc performance, plus the outstanding load drive capability, results in an exceptionally versatile amplifier for the single supply user.

The AD822 is available in four performance grades. The A and B grades are rated over the industrial temperature range of –40°C to +85°C. There is also a 3 volt grade—the AD822A-3V, rated over the industrial temperature range. The mil grade is rated over the military temperature range of –55°C to +125°C and is available processed on standard military drawing.

The AD822 is offered in three varieties of 8-pin package: plastic DIP, hermetic cerdip and surface mount (SOIC) as well as die form.



Input Voltage Noise vs. Frequency



Gain of +2 Amplifier; V_S = +5, 0, V_{IN} = 2.5 V Sine Centered at 1.25 Volts, R_L = 100 kΩ

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD822—SPECIFICATIONS (V_S = 0, 5 volts @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise noted)

Parameter	Conditions	AD822A Min	AD822A Typ	AD822A Max	AD822B Min	AD822B Typ	AD822B Max	AD822S[1] Min	AD822S[1] Typ	AD822S[1] Max	Units
DC PERFORMANCE											
Initial Offset			0.1	0.8		0.1	0.4		0.1	0.8	mV
Max Offset over Temperature			0.5	1.2		0.5	0.9		0.5		mV
Offset Drift			2			2			2		μV/°C
Input Bias Current	V_{CM} = 0 V to 4 V		2	25		2	10		2	25	pA
at T_{MAX}			0.5	5		0.5	2.5		0.5		nA
Input Offset Current			2	20		2	10		2	20	pA
at T_{MAX}			0.5			0.5			1.5		nA
Open-Loop Gain	V_O = 0.2 V to 4 V										
	R_L = 100 k	500	1000		500	1000		500	1000		V/mV
T_{MIN} to T_{MAX}		400			400						V/mV
	R_L = 10 k	80	150		80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80						V/mV
	R_L = 1 k	15	30		15	30		15	30		V/mV
T_{MIN} to T_{MAX}		10			10						V/mV
NOISE/HARMONIC PERFORMANCE											
Input Voltage Noise											
0.1 Hz to 10 Hz			2			2			2		μV p-p
f = 10 Hz			25			25			25		nV/√Hz
f = 100 Hz			21			21			21		nV/√Hz
f = 1 kHz			16			16			16		nV/√Hz
f = 10 kHz			13			13			13		nV/√Hz
Input Current Noise											
0.1 Hz to 10 Hz			18			18			18		fA p-p
f = 1 kHz			0.8			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10 k to 2.5 V										
f = 10 kHz	V_O = 0.25 V to 4.75 V		–93			–93			–93		dB
DYNAMIC PERFORMANCE											
Unity Gain Frequency			1.8			1.8			1.8		MHz
Full Power Response	V_O p-p = 4.5 V		210			210			210		kHz
Slew Rate			3			3			3		V/μs
Settling Time											
to 0.1%	V_O = 0.2 V to 4.5 V		1.4			1.4			1.4		μs
to 0.01%			1.8			1.8			1.8		μs
MATCHING CHARACTERISTICS											
Initial Offset				1.0			0.5			1.6	mV
Max Offset Over Temperature				1.6			1.3				mV
Offset Drift			3			3					μV/°C
Input Bias Current				20			10			20	pA
Crosstalk @ f = 1 kHz	R_L = 5 kΩ		–130			–130			–130		dB
f = 100 kHz			–93			–93			–93		dB
INPUT CHARACTERISTICS											
Common-Mode Voltage Range[2]		–0.2		4	–0.2		4	–0.2		4	V
T_{MIN} to T_{MAX}		–0.2		4	–0.2		4				V
CMRR	V_{CM} = 0 V to +2 V	66	80		69	80		66	80		dB
T_{MIN} to T_{MAX}		66			66						dB
Input Impedance											
Differential			10^{13}‖0.5			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF
OUTPUT CHARACTERISTICS											
Output Saturation Voltage[3]											
V_{OL}–V_{EE}	I_{SINK} = 20 μA		5	7		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10				mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 μA		10	14		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20				mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80				mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160				mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000				mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900				mV
Operating Output Current		15			15			15			mA
T_{MIN} to T_{MAX}		12			12						mA
Capacitive Load Drive			350			350			350		pF
POWER SUPPLY											
Quiescent Current T_{MIN} to T_{MAX}			1.24	1.6		1.24	1.6		1.24		mA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		66	80		70	80		dB
T_{MIN} to T_{MAX}		70			66						dB

(V_S = ±5 volts @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0 V unless otherwise noted)

Parameter	Conditions	AD822A			AD822B			AD822S[1]			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DC PERFORMANCE											
Initial Offset			0.1	0.8		0.1	0.4		0.1		mV
Max Offset over Temperature			0.5	1.5		0.5	1		0.5		mV
Offset Drift			2			2			2		µV/°C
Input Bias Current	V_{CM} = –5 V to 4 V		2	25		2	10		2	25	pA
at T_{MAX}			0.5	5		0.5	2.5		0.5		nA
Input Offset Current			2	20		2	10		2		pA
at T_{MAX}			0.5			0.5			1.5		nA
Open-Loop Gain	V_O = –4 V to 4 V										
	R_L = 100 k	400	1000		400	1000		400	1000		V/mV
T_{MIN} to T_{MAX}		400			400						V/mV
	R_L = 10 k	80	150		80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80						V/mV
	R_L = 1 k	20	30		20	30		20	30		V/mV
T_{MIN} to T_{MAX}		10			10						V/mV
NOISE/HARMONIC PERFORMANCE											
Input Voltage Noise											
0.1 Hz to 10 Hz			2			2			2		µV p-p
f = 10 Hz			25			25			25		nV/√Hz
f = 100 Hz			21			21			21		nV/√Hz
f = 1 kHz			16			16			16		nV/√Hz
f = 10 kHz			13			13			13		nV/√Hz
Input Current Noise											
0.1 Hz to 10 Hz			18			18			18		fA p-p
f = 1 kHz			0.8			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10 k										
f = 10 kHz	V_O = ±4.5 V		–93			–93			–93		dB
DYNAMIC PERFORMANCE											
Unity Gain Frequency			1.9			1.9			1.9		MHz
Full Power Response	V_O p-p = 9 V		105			105			105		kHz
Slew Rate			3			3			3		V/µs
Settling Time											
to 0.1%	V_O = 0 V to ±4.5 V		1.4			1.4			1.4		µs
to 0.01%			1.8			1.8			1.8		µs
MATCHING CHARACTERISTICS											
Initial Offset				1.0			0.5			1.6	mV
Max Offset Over Temperature				3			2			2	mV
Offset Drift			3			3					µV/°C
Input Bias Current				25			10			25	pA
Crosstalk @ f = 1 kHz	R_L = 5 kΩ		–130			–130			–130		dB
f = 100 kHz			–93			–93			–93		dB
INPUT CHARACTERISTICS											
Common-Mode Voltage Range[2]		–5.2		4	–5.2		4	–5.2		4	V
T_{MIN} to T_{MAX}		–5.2		4	–5.2		4				V
CMRR	V_{CM} = –5 V to +2 V	66	80		69	80		66	80		dB
T_{MIN} to T_{MAX}		66			66						dB
Input Impedance											
Differential			10^{13}‖0.5			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF
OUTPUT CHARACTERISTICS											
Output Saturation Voltage[3]											
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10				mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20				mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80				mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160				mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000				mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900				mV
Operating Output Current		15			15			15			mA
T_{MIN} to T_{MAX}		12			12						mA
Capacitive Load Drive			350			350			350		pF
POWER SUPPLY											
Quiescent Current T_{MIN} to T_{MAX}			1.3	1.6		1.3	1.6		1.3		mA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		66	80		70	80		dB
T_{MIN} to T_{MAX}		70			66						dB

AD822–SPECIFICATIONS (V_S = ±15 volts @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0 V unless otherwise noted)

		AD822A			AD822B			AD822S[1]			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
DC PERFORMANCE											
Initial Offset			0.4	2		0.3	1.5		0.4	2.0	mV
Max Offset over Temperature			0.5	3		0.5	2.5		0.5		mV
Offset Drift			2			2			2		μV/°C
Input Bias Current	V_{CM} = 0 V		2	25		2	12		2	25	pA
	V_{CM} = –10 V		40			40			40		pA
at T_{MAX}	V_{CM} = 0 V		0.5	5		0.5	2.5		0.5		nA
Input Offset Current			2	20		2	12		2	20	pA
at T_{MAX}			0.5			0.5			1.5		nA
Open-Loop Gain	V_O = +10 V to –10 V										
	R_L = 100 k	500	2000		500	2000		500	2000		V/mV
T_{MIN} to T_{MAX}		500			500						V/mV
	R_L = 10 k	100	500		100	500		150	400		V/mV
T_{MIN} to T_{MAX}		100			100						V/mV
	R_L = 1 k	30	45		30	45		30	45		V/mV
T_{MIN} to T_{MAX}		20			20						V/mV
NOISE/HARMONIC PERFORMANCE											
Input Voltage Noise											
0.1 Hz to 10 Hz			2			2			2		μV p-p
f = 10 Hz			25			25			25		$nV/\sqrt{Hz}$
f = 100 Hz			21			21			21		$nV/\sqrt{Hz}$
f = 1 kHz			16			16			16		$nV/\sqrt{Hz}$
f = 10 kHz			13			13			13		$nV/\sqrt{Hz}$
Input Current Noise											
0.1 Hz to 10 Hz			18			18			18		fA p-p
f = 1 kHz			0.8			0.8			0.8		$fA/\sqrt{Hz}$
Harmonic Distortion	R_L = 10 k										
f = 10 kHz	V_O = ±10 V		–85			–85			–85		dB
DYNAMIC PERFORMANCE											
Unity Gain Frequency			1.9			1.9			1.9		MHz
Full Power Response	V_O p-p = 20 V		45			45			45		kHz
Slew Rate			3			3			3		V/μs
Settling Time											
to 0.1%	V_O = 0 V to ±10 V		4.1			4.1			4.1		μs
to 0.01%			4.5			4.5			4.5		μs
MATCHING CHARACTERISTICS											
Initial Offset				3			2			0.8	mV
Max Offset Over Temperature				4			2.5			1.0	mV
Offset Drift			3			3					μV/°C
Input Bias Current				25			12			25	pA
Crosstalk @ f = 1 kHz	R_L = 5 kΩ		–130			–130			–130		dB
f = 100 kHz			–93			–93			–93		dB
INPUT CHARACTERISTICS											
Common-Mode Voltage Range[2]		–15.2		14	–15.2		14	–15.2		14	V
T_{MIN} to T_{MAX}		–15.2		14	–15.2		14				V
CMRR	V_{CM} = –15 V to 12 V	70	80		74	90		70	90		dB
T_{MIN} to T_{MAX}		70			74						dB
Input Impedance											
Differential			10^{13}‖0.5			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF
OUTPUT CHARACTERISTICS											
Output Saturation Voltage[3]											
$V_{OL}–V_{EE}$	I_{SINK} = 20 μA		5	7		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10				mV
$V_{CC}–V_{OH}$	I_{SOURCE} = 20 μA		10	14		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20				mV
$V_{OL}–V_{EE}$	I_{SINK} = 2 mA		40	55		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80				mV
$V_{CC}–V_{OH}$	I_{SOURCE} = 2 mA		80	110		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160				mV
$V_{OL}–V_{EE}$	I_{SINK} = 15 mA		300	500		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000				mV
$V_{CC}–V_{OH}$	I_{SOURCE} = 15 mA		800	1500		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900				mV
Operating Output Current		20			20			20			mA
T_{MIN} to T_{MAX}		15			15						mA
Capacitive Load Drive			350			350			350		pF
POWER SUPPLY											
Quiescent Current T_{MIN} to T_{MAX}			1.4	1.8		1.4	1.8		1.4		mA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		70	80		70	80		dB
T_{MIN} to T_{MAX}		70			70						dB

(V_S = 0, 3 volts @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise noted)

Parameter	Conditions	AD822A-3 V Min	Typ	Max	Units
DC PERFORMANCE					
Initial Offset			0.2	1	mV
Max Offset over Temperature			0.5	1.5	mV
Offset Drift			1		μV/°C
Input Bias Current	V_{CM} = 0 V to +2 V		2	25	pA
at T_{MAX}			0.5	5	nA
Input Offset Current			2	20	pA
at T_{MAX}			0.5		nA
Open-Loop Gain	V_O = 0.2 V to 2 V				
	R_L = 100 k	300	1000		V/mV
T_{MIN} to T_{MAX}		300			V/mV
	R_L = 10 k	60	150		V/mV
T_{MIN} to T_{MAX}		60			V/mV
	R_L = 1 k	10	30		V/mV
T_{MIN} to T_{MAX}		8			V/mV
NOISE/HARMONIC PERFORMANCE					
Input Voltage Noise					
0.1 Hz to 10 Hz			2		μV p-p
f = 10 Hz			25		nV/√Hz
f = 100 Hz			21		nV/√Hz
f = 1 kHz			16		nV/√Hz
f = 10 kHz			13		nV/√Hz
Input Current Noise					
0.1 Hz to 10 Hz			18		fA p-p
f = 1 kHz			0.8		fA/√Hz
Harmonic Distortion	R_L = 10 k to 1.5 V				
f = 10 kHz	V_O = ±1.25 V		–92		dB
DYNAMIC PERFORMANCE					
Unity Gain Frequency			1.5		MHz
Full Power Response	V_O p-p = 2.5 V		240		kHz
Slew Rate			3		V/μs
Settling Time					
to 0.1%	V_O = 0.2 V to 2.5 V		1		μs
to 0.01%			1.4		μs
MATCHING CHARACTERISTICS					
Initial Offset				1	mV
Max Offset Over Temperature				2	mV
Offset Drift			2		μV/°C
Input Bias Current				10	pA
Crosstalk @ f = 1 kHz	R_L = 5 kΩ		–130		dB
f = 100 kHz			–93		dB
INPUT CHARACTERISTICS					
Common-Mode Voltage Range[2]		–0.2		2	V
T_{MIN} to T_{MAX}		–0.2		2	V
CMRR	V_{CM} = 0 V to +1 V	60	74		dB
T_{MIN} to T_{MAX}		60			dB
Input Impedance					
Differential			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8		Ω‖pF
OUTPUT CHARACTERISTICS					
Output Saturation Voltage[3]					
V_{OL}–V_{EE}	I_{SINK} = 20 μA		5	7	mV
T_{MIN} to T_{MAX}				10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 μA		10	14	mV
T_{MIN} to T_{MAX}				20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55	mV
T_{MIN} to T_{MAX}				80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110	mV
T_{MIN} to T_{MAX}				160	mV
V_{OL}–V_{EE}	I_{SINK} = 10 mA		200	400	mV
T_{MIN} to T_{MAX}				400	mV
V_{CC}–V_{OH}	I_{SOURCE} = 10 mA		500	1000	mV
T_{MIN} to T_{MAX}				1000	mV
Operating Output Current		15			mA
T_{MIN} to T_{MAX}		12			mA
Capacitive Load Drive			350		pF
POWER SUPPLY					
Quiescent Current T_{MIN} to T_{MAX}			1.24	1.6	mA
Power Supply Rejection	V_S+ = 3 V to 15 V	70	80		dB
T_{MIN} to T_{MAX}		70			dB

NOTES
[1]See standard military drawing for 883B specifications.
[2]This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range ($+V_S$ – 1 V) to $+V_S$. Common-mode error voltage is typically less than 5 mV with the common-mode voltage set at 1 volt below the positive supply.
[3]$V_{OL}–V_{EE}$ is defined as the difference between the lowest possible output voltage (V_{OL}) and the minus voltage supply rail (V_{EE}). $V_{CC}–V_{OH}$ is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).

Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD822 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation
  Plastic DIP (N) . . . . Observe Derating Curves
  Cerdip (Q) . . . . Observe Derating Curves
  SOIC (R) . . . . Observe Derating Curves
Input Voltage . . . . ($+V_S$ + 0.2 V) to –(20 V + V_S)
Output Short Circuit Duration . . . . Indefinite
Differential Input Voltage . . . . ±30 V
Storage Temperature Range (N) . . . . –65°C to +125°C
Storage Temperature Range (Q) . . . . –65°C to +150°C
Storage Temperature Range (R) . . . . –65°C to +150°C
Operating Temperature Range
  AD822A/B . . . . –40°C to +85°C
  AD822S . . . . –55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . +260°C

NOTES
[1]Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic DIP Package: θ_{JA} = 90°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin SOIC Package: θ_{JA} = 160°C/Watt

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD822 is limited by the associated rise in junction temperature. For plastic packages, the maximum safe junction temperature is 145°C. For the cerdip packages, the maximum junction temperature is 175°C. If these maximums are exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the “overheated” condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the derating curves shown in Figure 24.

While the AD822 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. With power supplies ±12 volts (or less) at an ambient temperature of +25°C or less, if the output node is shorted to a supply rail, then the amplifier will not be destroyed, even if this condition persists for an extended period.

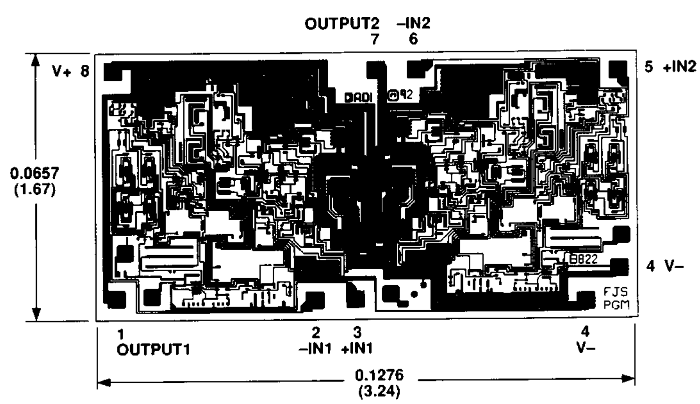
ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD822AN	–40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD822BN	–40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD822AR	–40°C to +85°C	8-Pin SOIC	R-8
AD822BR	–40°C to +85°C	8-Pin SOIC	R-8
AD822AR-3V	–40°C to +85°C	8-Pin SOIC	R-8
AD822AN-3V	–40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD822A Chips	–40°C to +85°C	Die	
Standard Military Drawing[2]	–55°C to +125°C	8-Pin Cerdip	Q-8

NOTES
[1]Spice model is available on ADI Model Disc.
[2]Contact factory for availability.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



NOTE: BACK OF DIE IS AT $+V_S$ POTENTIAL.

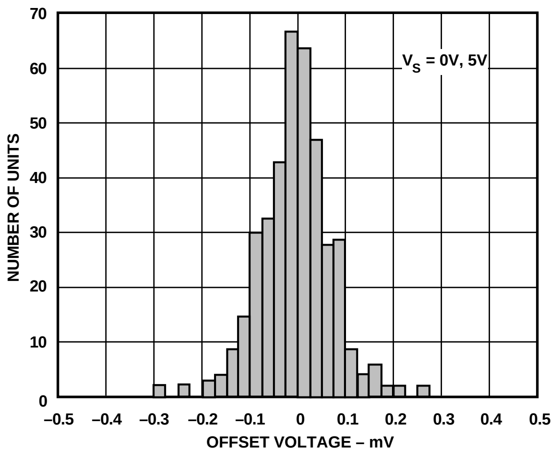


Figure 1. Typical Distribution of Offset Voltage (390 Units)

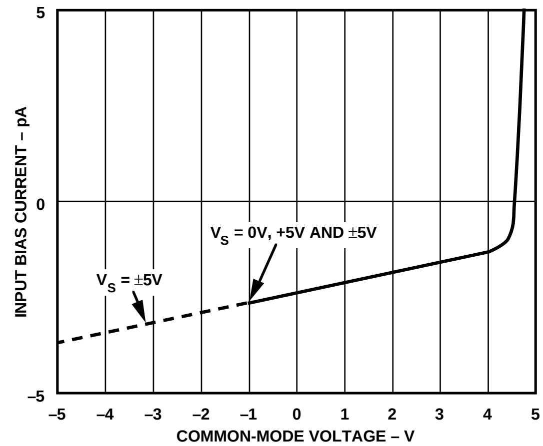


Figure 4. Input Bias Current vs. Common-Mode Voltage; V_S = +5 V, 0 V and V_S = ±5 V

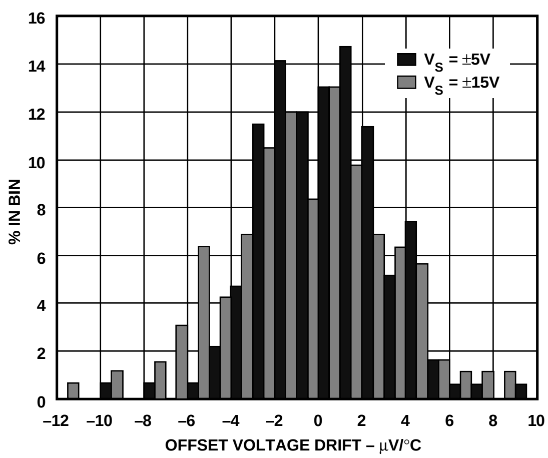


Figure 2. Typical Distribution of Offset Voltage Drift (100 Units)

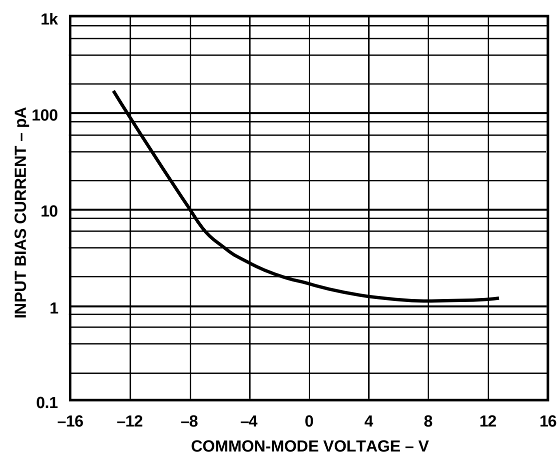


Figure 5. Input Bias Current vs. Common-Mode Voltage; V_S = ±15 V

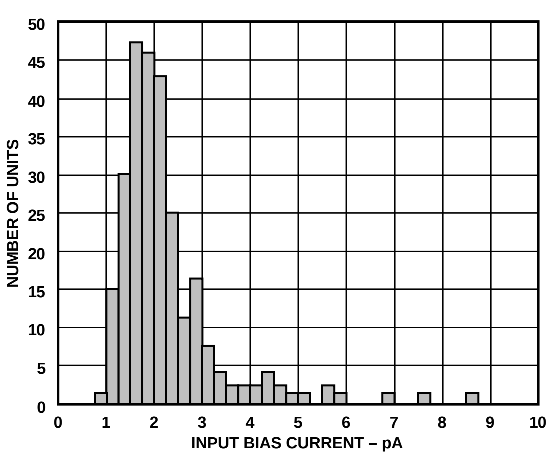


Figure 3. Typical Distribution of Input Bias Current (213 Units)

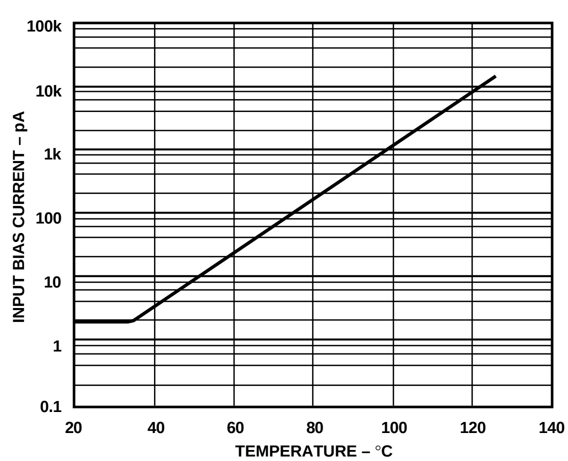


Figure 6. Input Bias Current vs. Temperature; V_S = 5 V, V_{CM} = 0

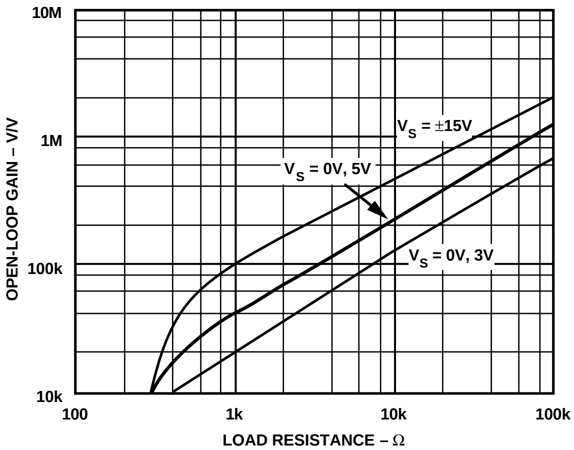


Figure 7. Open-Loop Gain vs. Load Resistance

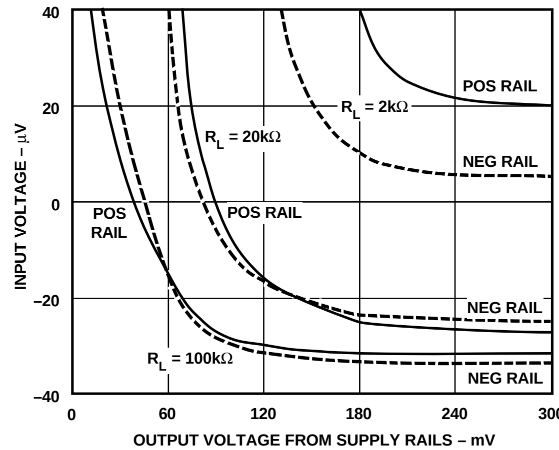


Figure 10. Input Error Voltage with Output Voltage within 300 mV of Either Supply Rail for Various Resistive Loads; $V_S = \pm 5$ V

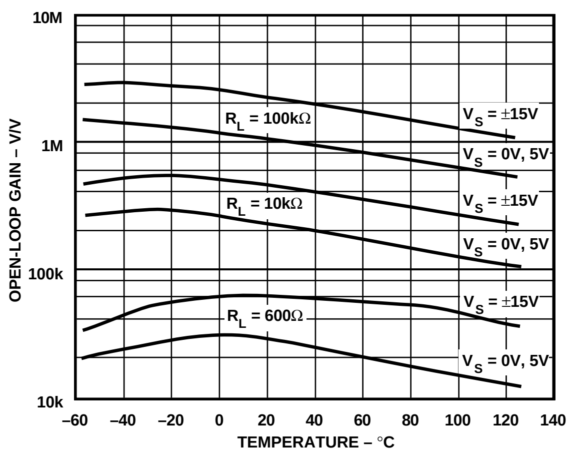


Figure 8. Open-Loop Gain vs. Temperature

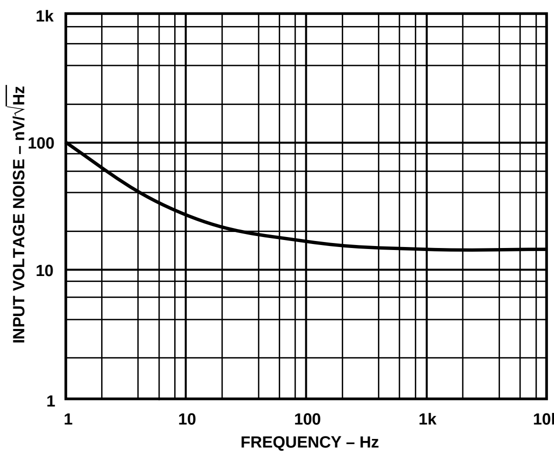


Figure 11. Input Voltage Noise vs. Frequency

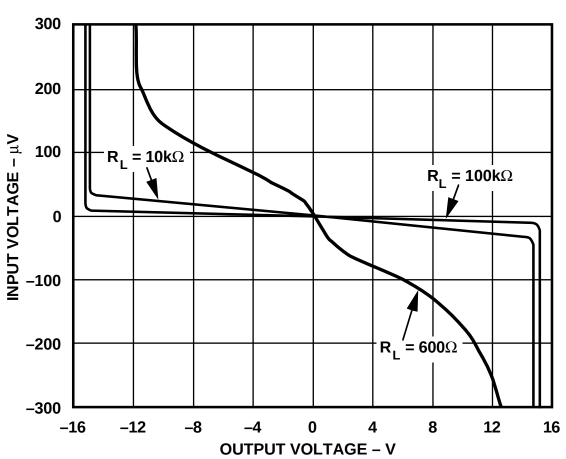


Figure 9. Input Error Voltage vs. Output Voltage for Resistive Loads

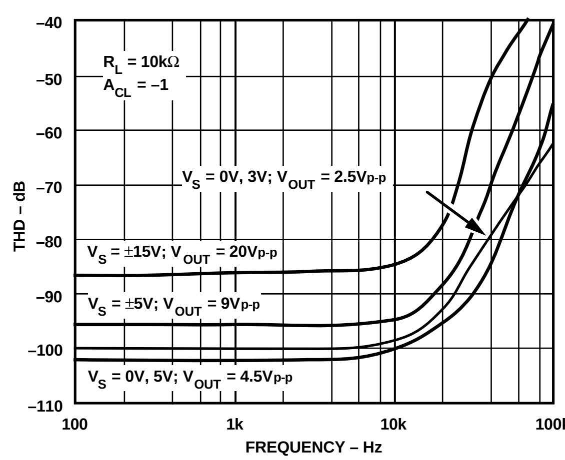


Figure 12. Total Harmonic Distortion vs. Frequency

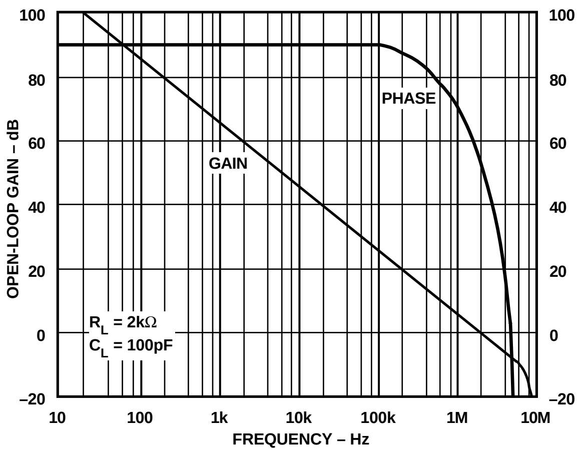


Figure 13. Open-Loop Gain and Phase Margin vs. Frequency

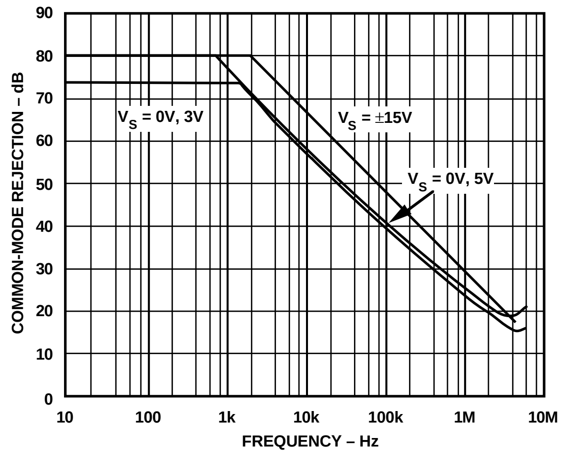


Figure 16. Common-Mode Rejection vs. Frequency

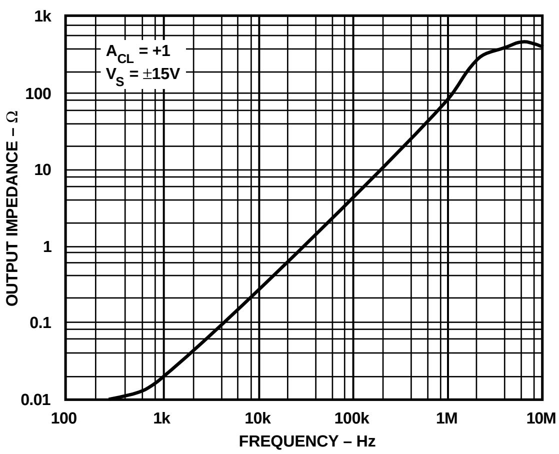


Figure 14. Output Impedance vs. Frequency

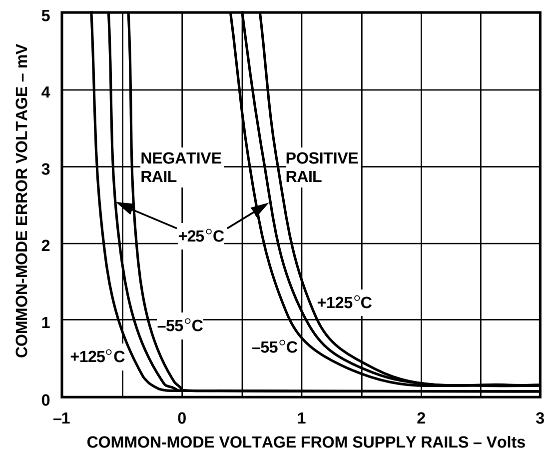


Figure 17. Absolute Common-Mode Error vs. Common-Mode Voltage from Supply Rails ($V_S - V_{CM}$)

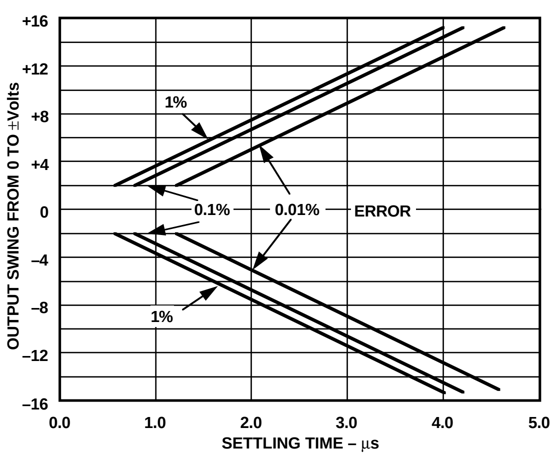


Figure 15. Output Swing and Error vs. Settling Time

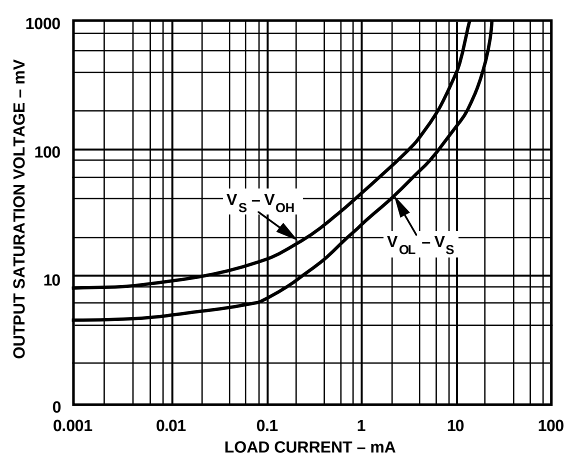


Figure 18. Output Saturation Voltage vs. Load Current

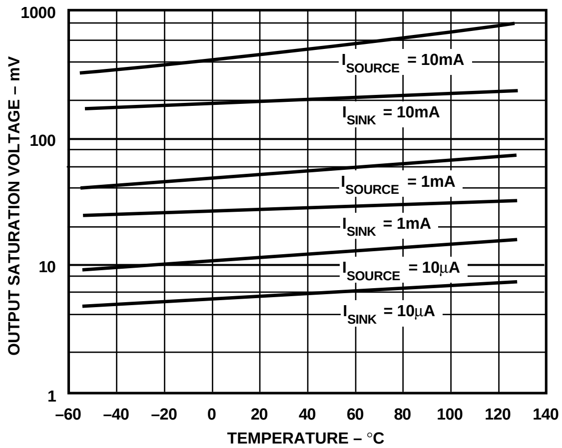


Figure 19. Output Saturation Voltage vs. Temperature

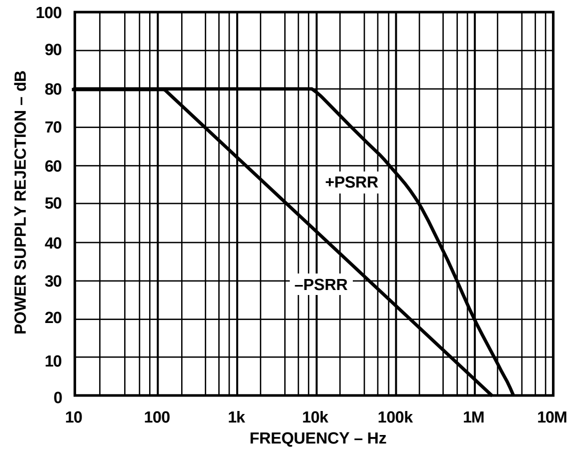


Figure 22. Power Supply Rejection vs. Frequency

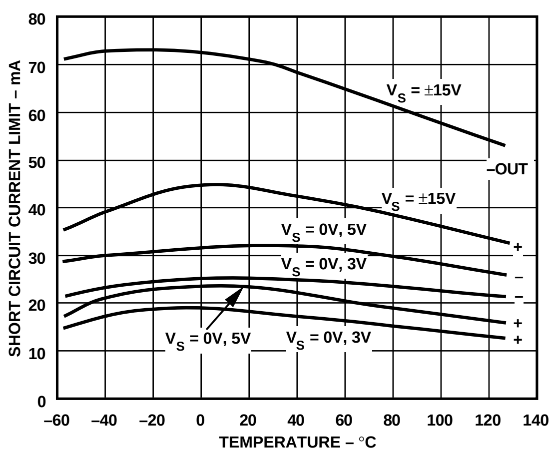


Figure 20. Short Circuit Current Limit vs. Temperature

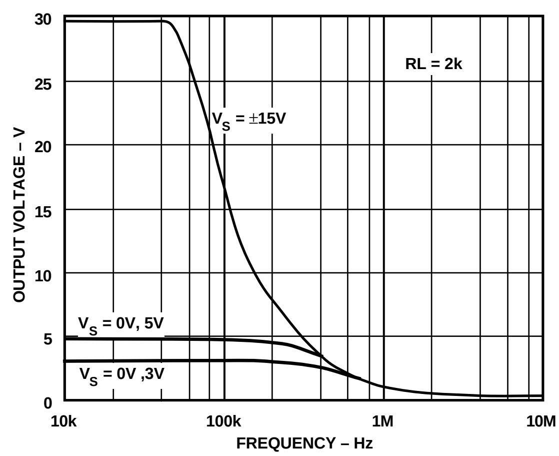


Figure 23. Large Signal Frequency Response

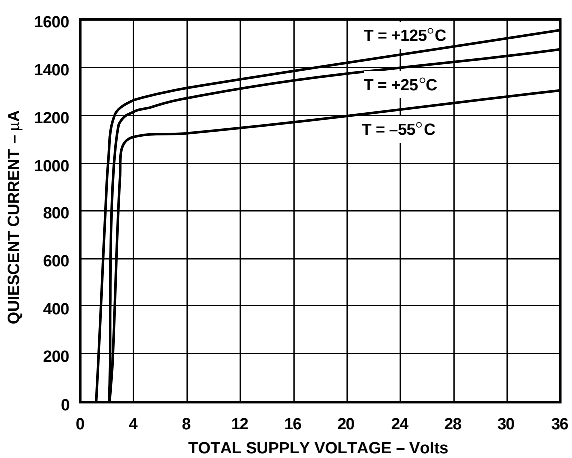


Figure 21. Quiescent Current vs. Supply Voltage vs. Temperature

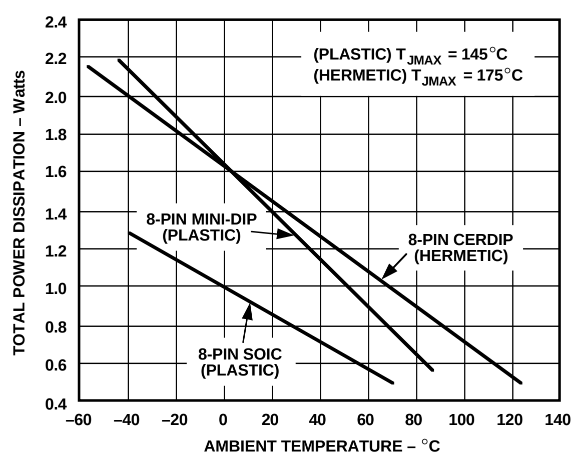


Figure 24. Maximum Power Dissipation vs. Temperature for Plastic and Hermetic Packages

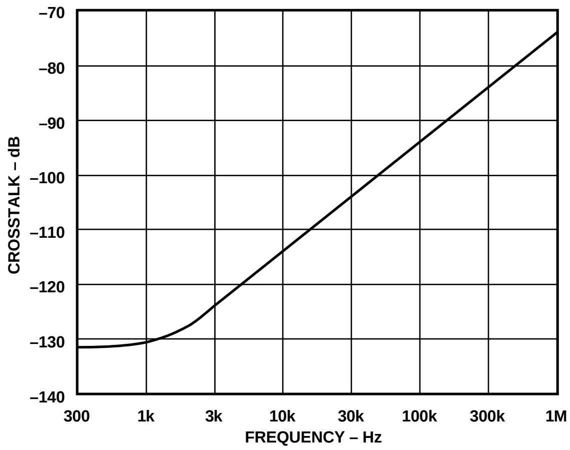


Figure 25. Crosstalk vs. Frequency

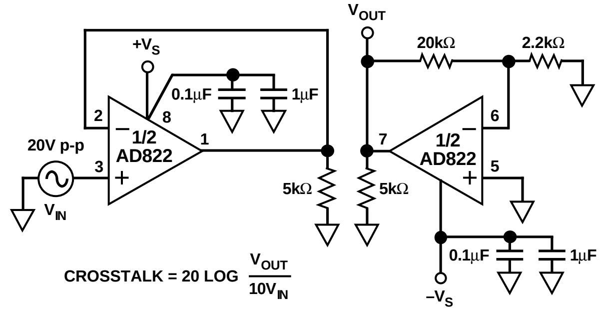


Figure 28. Crosstalk Test Circuit

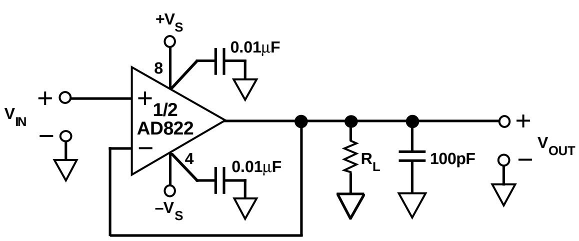


Figure 26. Unity-Gain Follower

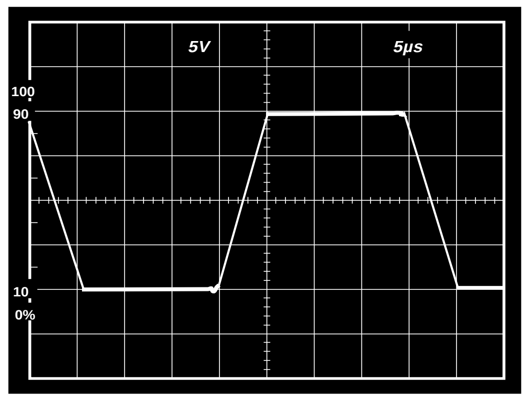


Figure 29. Large Signal Response Unity Gain Follower; $V_S = \pm 15$ V, $R_L = 10$ kΩ

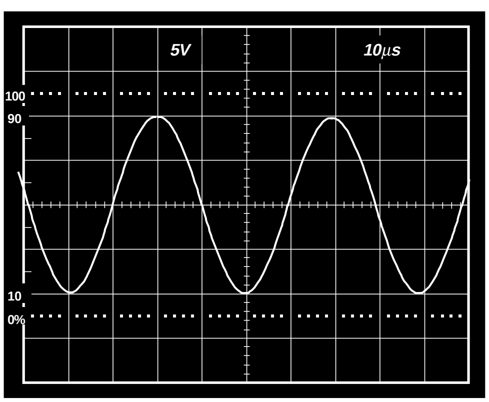


Figure 27. 20 V p-p, 25 kHz Sine Wave Input; Unity Gain Follower; $R_L = 600\ \Omega$, $V_S = \pm 15$ V

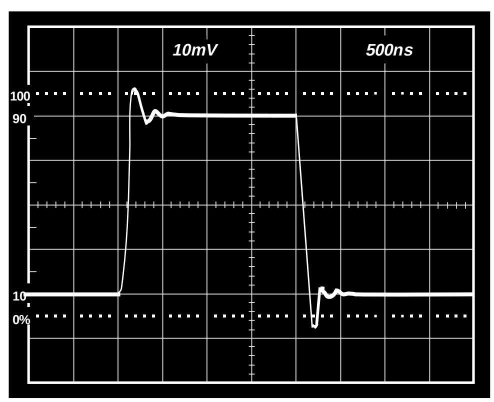


Figure 30. Small Signal Response Unity Gain Follower; $V_S = \pm 15$ V, $R_L = 10$ kΩ

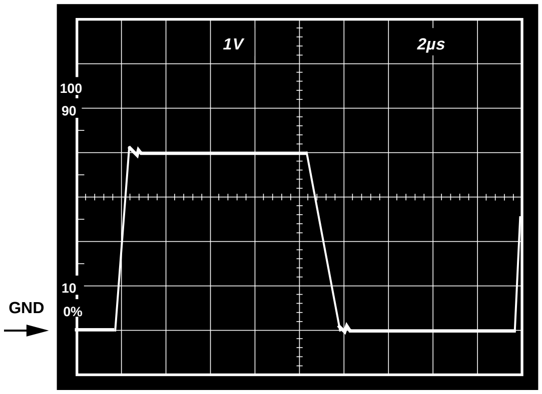


Figure 31. V_S = +5 V, 0 V; Unity Gain Follower Response to 0 V to 4 V Step

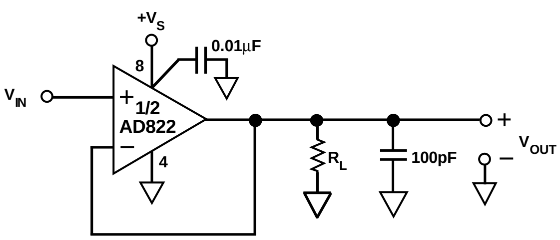


Figure 32. Unity Gain Follower

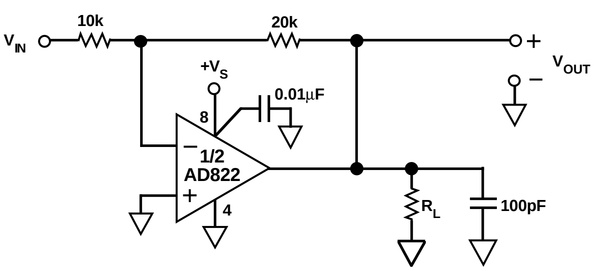


Figure 33. Gain of Two Inverter

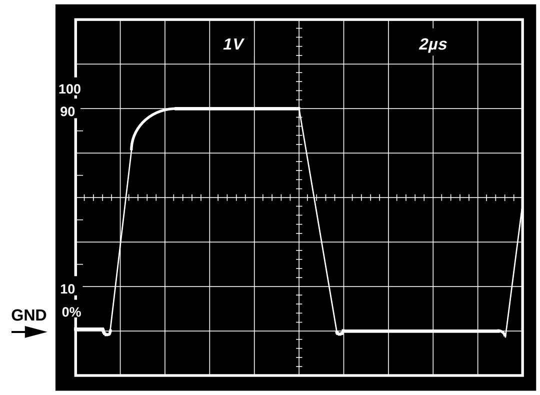


Figure 34. V_S = +5 V, 0 V; Unity Gain Follower Response to 0 V to 5 V Step

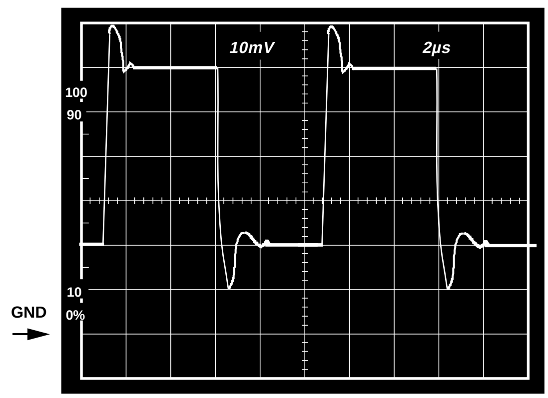


Figure 35. V_S = +5 V, 0 V; Unity Gain Follower Response, to 40 mV Step Centered 40 mV Above Ground, R_L = 10 kΩ

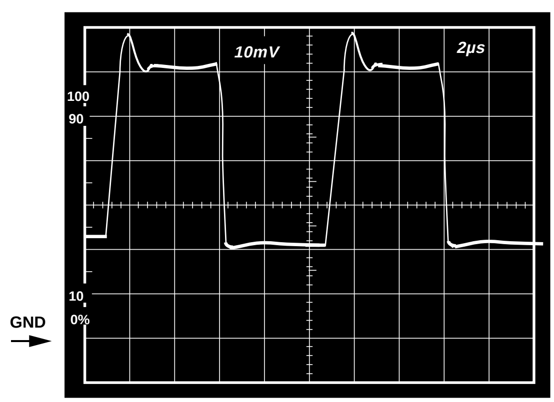


Figure 36. V_S = +5 V, 0 V; Gain of Two Inverter Response to 20 mV Step, Centered 20 mV Below Ground, R_L = 10 kΩ

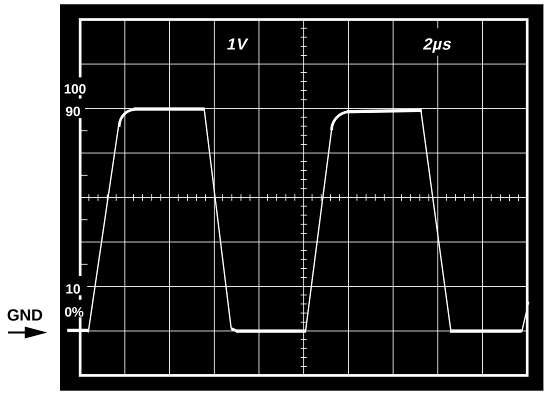


Figure 37. V_S = +5 V, 0 V; Gain of Two Inverter Response to 2.5 V Step Centered –1.25 V Below Ground, R_L = 10 kΩ

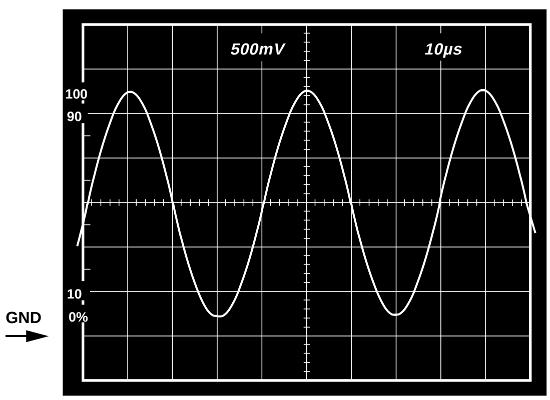


Figure 38. V_S = 3 V, 0 V; Gain of Two Inverter, V_{IN} = 1.25 V, 25 kHz, Sine Wave Centered at –0.75 V, R_L = 600 Ω

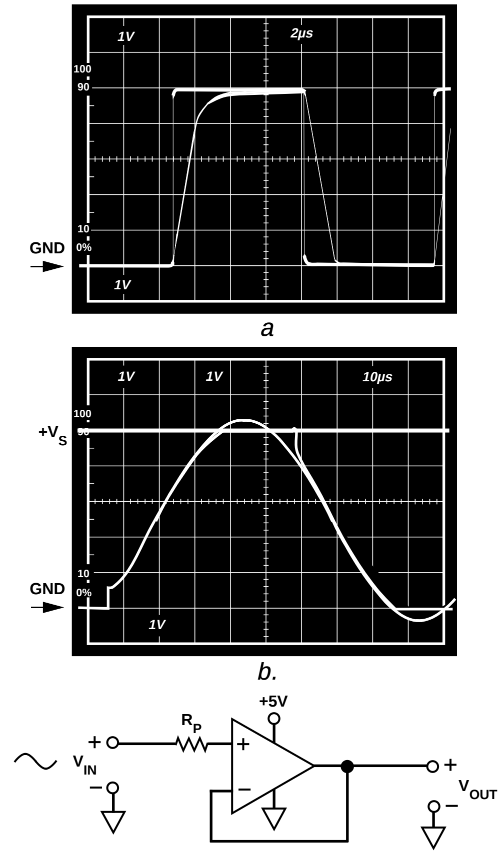


Figure 39. (a) Response with R_P = 0; V_{IN} from 0 to $+V_S$
(b) V_{IN} = 0 to $+V_S$ + 200 mV
V_{OUT} = 0 to $+V_S$
R_P = 49.9 kΩ

APPLICATION NOTES

INPUT CHARACTERISTICS

In the AD822, n-channel JFETs are used to provide a low offset, low noise, high impedance input stage. Minimum input common-mode voltage extends from 0.2 V below $–V_S$ to 1 V less than $+V_S$. Driving the input voltage closer to the positive rail will cause a loss of amplifier bandwidth (as can be seen by comparing the large signal responses shown in Figures 31 and 34) and increased common-mode voltage error as illustrated in Figure 17.

The AD822 does not exhibit phase reversal for input voltages up to and including $+V_S$. Figure 39a shows the response of an AD822 voltage follower to a 0 V to +5 V ($+V_S$) square wave input. The input and output arc superimposed. The output tracks the input up to $+V_S$ without phase reversal. The reduced bandwidth above a 4 V input causes the rounding of the output wave form. For input voltages greater than $+V_S$, a resistor in series with the AD822's noninverting input will prevent phase reversal, at the expense of greater input voltage noise. This is illustrated in Figure 39b.

Since the input stage uses n-channel JFETs, input current during normal operation is negative; the current flows out from the input terminals. If the input voltage is driven more positive than $+V_S$ – 0.4 V, the input current will reverse direction as internal device junctions become forward biased. This is illustrated in Figure 4.

A current limiting resistor should be used in series with the input of the AD822 if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV, or if an input voltage will be applied to the AD822 when $\pm V_S$ = 0. The amplifier will be damaged if left in that condition for more than 10 seconds. A 1 kΩ resistor allows the amplifier to withstand up to 10 volts of continuous overvoltage, and increases the input voltage noise by a negligible amount.

Input voltages less than $–V_S$ are a completely different story. The amplifier can safely withstand input voltages 20 volts below the minus supply voltage as long as the total voltage from the positive supply to the input terminal is less than 36 volts. In addition, the input stage typically maintains picoamp level input currents across that input voltage range.

The AD822 is designed for 13 nV/√Hz wideband input voltage noise and maintains low noise performance to low frequencies (refer to Figure 11). This noise performance, along with the AD822's low input current and current noise means that the AD822 contributes negligible noise for applications with source resistances greater than 10 kΩ and signal bandwidths greater than 1 kHz. This is illustrated in Figure 40.

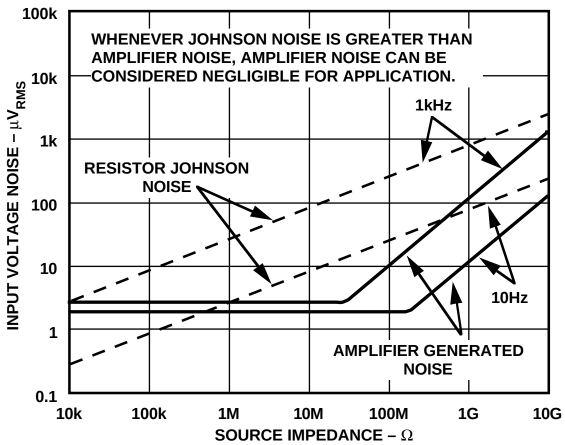


Figure 40. Total Noise vs. Source Impedance

OUTPUT CHARACTERISTICS

The AD822 s unique bipolar rail-to-rail output stage swings within 5 mV of the minus supply and 10 mV of the positive supply with no external resistive load. The AD822's approximate output saturation resistance is 40 Ω sourcing and 20 Ω sinking. This can be used to estimate output saturation voltage when driving heavier current loads. For instance, when sourcing 5 mA, the saturation voltage to the positive supply rail will be 200 mV, when sinking 5 mA, the saturation voltage to the minus rail will be 100 mV.

The amplifier's open-loop gain characteristic will change as a function of resistive load, as shown in Figures 7 through 10. For load resistances over 20 kΩ, the AD822's input error voltage is virtually unchanged until the output voltage is driven to 180 mV of either supply.

If the AD822's output is overdriven so as to saturate either of the output devices, the amplifier will recover within 2 μs of its input returning to the amplifier's linear operating region.

Direct capacitive loads will interact with the amplifier's effective output impedance to form an additional pole in the amplifier's feedback loop, which can cause excessive peaking on the pulse response or loss of stability. Worst case is when the amplifier is used as a unity gain follower. Figure 41 shows the AD822's pulse response as a unity gain follower driving 350 pF. This amount of overshoot indicates approximately 20 degrees of phase margin—the system is stable, but is nearing the edge. Configurations with less loop gain, and as a result less loop bandwidth, will be much less sensitive to capacitance load effects. Figure 42 is a plot of capacitive load that will result in a 20 degree phase margin versus noise gain for the AD822. Noise gain is the inverse of the feedback attenuation factor provided by the feedback network in use.

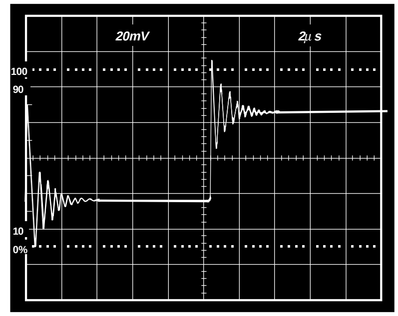


Figure 41. Small Signal Response of AD822 as Unity Gain Follower Driving 350 pF Capacitive Load

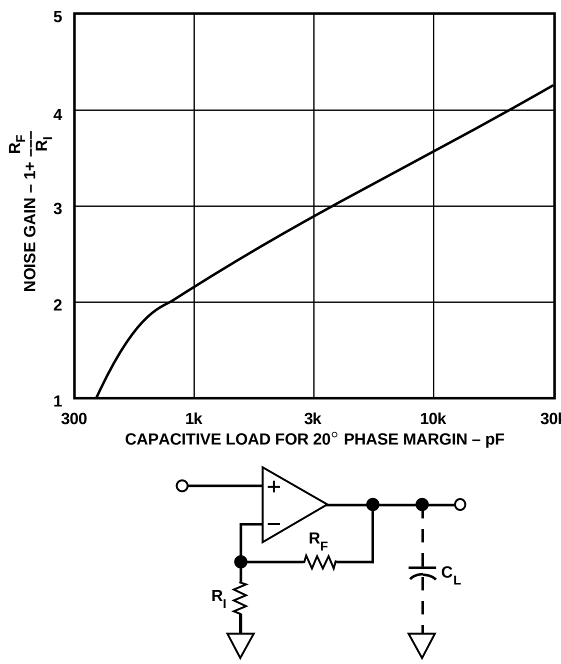


Figure 42. Capacitive Load Tolerance vs. Noise Gain

Figure 43 shows a method for extending capacitance load drive capability for a unity gain follower. With these component values, the circuit will drive 5,000 pF with a 10% overshoot.

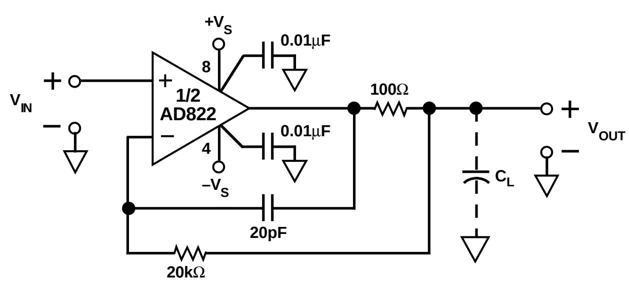


Figure 43. Extending Unity Gain Follower Capacitive Load Capability Beyond 350 pF

APPLICATIONS

Single Supply Voltage-to-Frequency Converter

The circuit shown in Figure 44 uses the AD822 to drive a low power timer, which produces a stable pulse of width t_1. The positive going output pulse is integrated by R1-C1 and used as one input to the AD822, which is connected as a differential integrator. The other input (nonloading) is the unknown voltage, V_{IN}. The AD822 output drives the timer trigger input, closing the overall feedback loop.

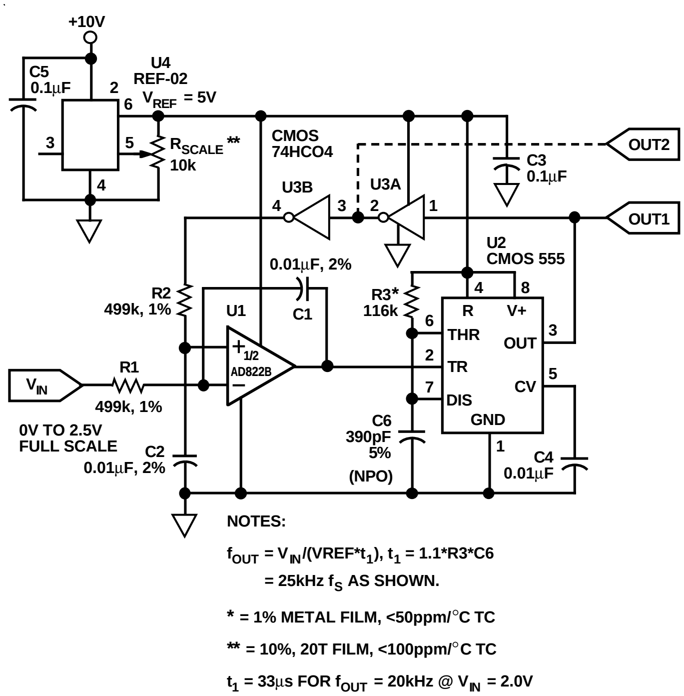


Figure 44. Single Supply Voltage-to-Frequency Converter

Typical AD822 bias currents of 2 pA allow megaohm-range source impedances with negligible dc errors. Linearity errors on the order of 0.01% full scale can be achieved with this circuit. This performance is obtained with a 5 volt single supply which delivers less than 1 mA to the entire circuit.

Single Supply Programmable Gain Instrumentation Amplifier

The AD822 can be configured as a single supply instrumentation amplifier that is able to operate from single supplies down to 3 V, or dual supplies up to ±15 V. Using only one AD822 rather than three separate op amps, this circuit is cost and power efficient. AD822 FET inputs' 2 pA bias currents minimize offset errors caused by high unbalanced source impedances.

An array of precision thin-film resistors sets the in amp gain to be either 10 or 100. These resistors are laser-trimmed to ratio match to 0.01%, and have a maximum differential TC of 5 ppm/°C.

Table I. AD822 In Amp Performance

Parameters	V_S = 3 V, 0 V	V_S = ±5 V
CMRR	74 dB	80 dB
Common-Mode Voltage Range	–0.2 V to +2 V	–5.2 V to +4 V
3 dB BW, G = 10	180 kHz	180 kHz
G = 100	18 kHz	18 kHz
$t_{SETTLING}$		
2 V Step (V_S = 0 V, 3 V)	2 µs	
5 V (V_S = ±5 V)		5 µs
Noise @ f = 1 kHz, G = 10	270 nV/√Hz	270 nV/√Hz
G = 100	2.2 µV/√Hz	2.2 µV/√Hz
I_{SUPPLY} (Total)	1.10 mA	1.15 mA

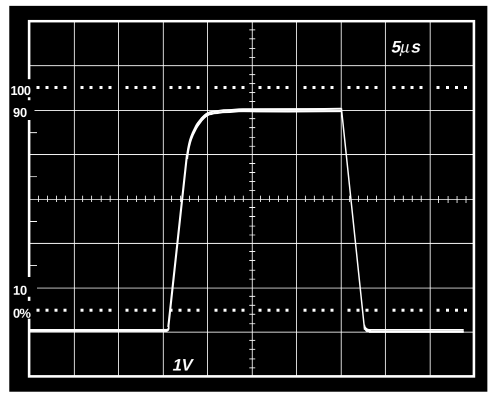


Figure 45a. Pulse Response of In Amp to a 500 mV p-p Input Signal; V_S = +5 V, 0 V; Gain = 10

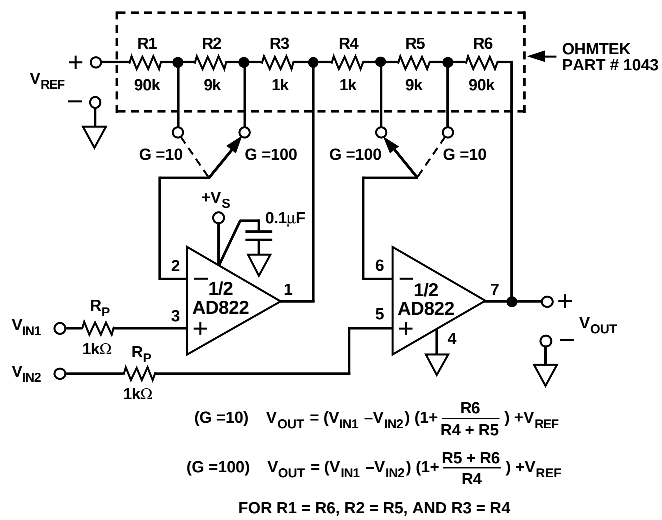


Figure 45b. A Single Supply Programmable Instrumentation Amplifier

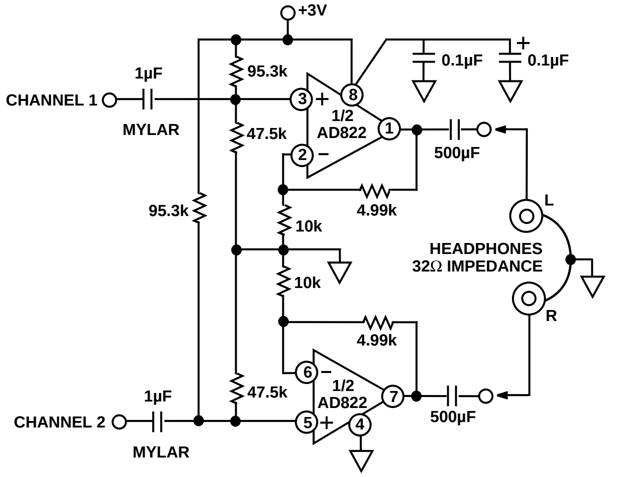


Figure 46. 3 Volt Single Supply Stereo Headphone Driver

3 Volt, Single Supply Stereo Headphone Driver

The AD822 exhibits good current drive and THD+N performance, even at 3 V single supplies. At 1 kHz, total harmonic distortion plus noise (THD+N) equals –62 dB (0.079%) for a 300 mV p-p output signal. This is comparable to other single supply op amps which consume more power and cannot run on 3 V power supplies.

In Figure 46, each channel s input signal is coupled via a 1 μF Mylar capacitor. Resistor dividers set the dc voltage at the noninverting inputs so that the output voltage is midway between the power supplies (+1.5 V). The gain is 1.5. Each half of the AD822 can then be used to drive a headphone channel. A 5 Hz high-pass filter is realized by the 500 μF capacitors and the headphones, which can be modeled as 32 ohm load resistors to ground. This ensures that all signals in the audio frequency range (20 Hz–20 kHz) are delivered to the headphones.

Low Dropout Bipolar Bridge Driver

The AD822 can be used for driving a 350 ohm Wheatstone bridge. Figure 47 shows one half of the AD822 being used to buffer the AD589—a 1.235 V low power reference. The output of +4.5 V can be used to drive an A/D converter front end. The other half of the AD822 is configured as a unity-gain inverter, and generates the other bridge input of –4.5 V. Resistors R1 and R2 provide a constant current for bridge excitation. The AD620 low power instrumentation amplifier is used to condition the differential output voltage of the bridge. The gain of the AD620 is programmed using an external resistor R_G, and determined by:

$$G = \frac{49.4\ k\Omega}{R_G} + 1$$

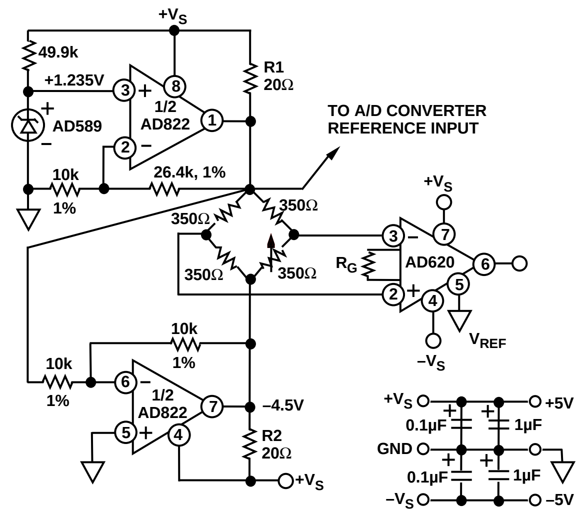
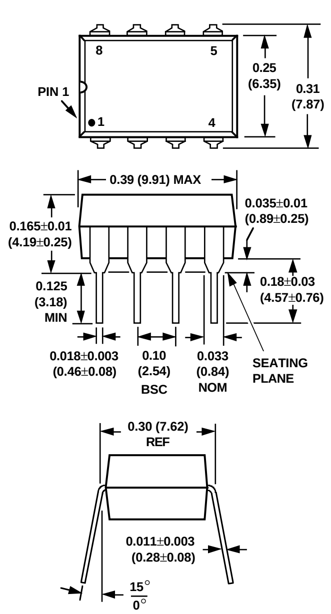


Figure 47. Low Dropout Bipolar Bridge Driver

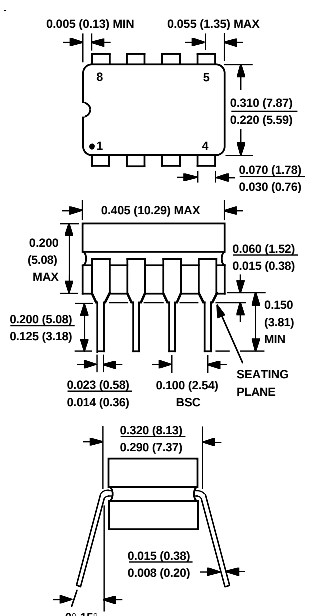
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

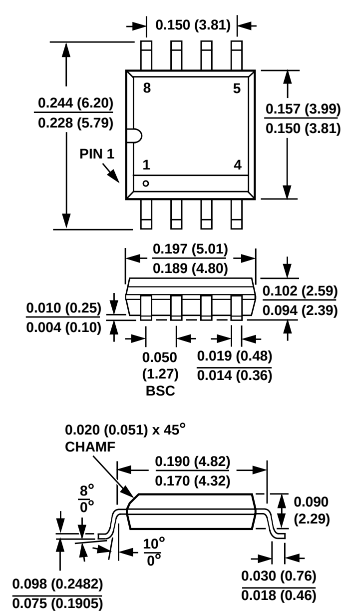
Mini-DIP (N) Package



Cerdip (Q) Package



SOIC (R) Package



C1821a–10–9/91

PRINTED IN U.S.A.